(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
11 January 2001 (11.01.2001)

PCT

(10) International Publication Number
WO 01/03188 A1

(51) International Patent Classification[7]: H01L 23/66, 23/64

(21) International Application Number: PCT/US99/22438

(22) International Filing Date:
28 September 1999 (28.09.1999)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/345,886 1 July 1999 (01.07.1999) US

(63) Related by continuation (CON) or continuation-in-part (CIP) to earlier application:
US 09/345,886 (CON)
Filed on 1 July 1999 (01.07.1999)

(71) Applicant *(for all designated States except US)*: **INTERMEC IP CORP.** [US/US]; 21900 Burbank Boulevard, Woodland Hills, CA 91367-7418 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **BRADY, Michael, John** [US/US]; 72 Seven Oak Lane, Brewster, NY 10509 (US). **DUAN, Dah-Weih** [CN/US]; 1185 Park Lane, Yorktown Heights, NY 10598 (US).

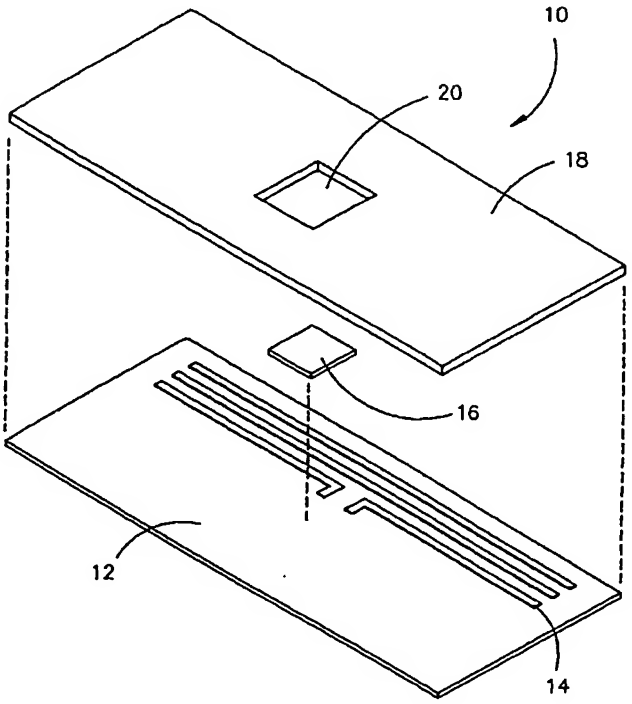
(74) Agents: **BERLINER, Brian, M.** et al.; O'Melveny & Myers LLP, 400 South Hope Street, Los Angeles, CA 90071-2899 (US).

(81) Designated States *(national)*: AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ZA, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU,

[Continued on next page]

(54) Title: INTEGRATED CIRCUIT ATTACHMENT PROCESS AND APPARATUS



(57) Abstract: A radio frequency transponder (10) comprises a substrate (12) having an electrically conductive material disposed thereon, and a superstrate (18) having an integrated circuit retention aperture. The superstrate is laminated to the substrate and substantially covers the electrically conductive material on the substrate. An integrated circuit (16) is substantially retained within the integrated circuit retention aperture and is operatively connected to the electrically conductive material. The substrate and superstrate may be each comprised of an organic material. The electrically conductive material comprises a metal material patterned to provide an antenna (14). An encapsulant material is disposed within the integrated circuit retention aperture substantially enclosing the integrated circuit therein. In another embodiment of the invention, an additional superstrate is provided on an opposite side of the substrate from the first superstrate. The substrate layer further includes a second integrated circuit retention aperture, and the integrated circuit is retained within both the first and second integrated circuit retention apertures. In yet another embodiment of the invention, the superstrate is laminated to the opposite side of the substrate only, and the integrated circuit retention aperture is provided in the substrate. Each of the embodiments of the invention provides a chip-in-cavity package having a relatively small form factor.

WO 01/03188 A1

MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published:

— *With international search report.*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

INTEGRATED CIRCUIT ATTACHMENT PROCESS AND APPARATUS

CROSS-REFERENCE TO RELATED APPLICATION

This application claims the benefit under 35 U.S.C. § 119(e) of U.S. Provisional Application Number 60/093,088, filed on July 16, 1998, which application is specifically incorporated by reference herein.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to radio frequency identification (RFID) systems, and more specifically to RFID systems having an improved form factor.

2. Description of Related Art

In the automatic data identification industry, the use of RFID transponders (also known as RFID tags) has grown in prominence as a way to track data regarding an object to which an RFID transponder is affixed. An RFID transponder generally includes a semiconductor memory in which information may be stored. An RFID interrogator containing a transmitter-receiver unit is used to query an RFID transponder that may be at a distance from the interrogator. The RFID transponder detects the interrogating signal and transmits a response signal containing encoded data back to the interrogator. RFID systems are used in applications such as inventory management, security access, personnel identification, factory automation, automotive toll debiting, and vehicle identification, to name just a few.

Such RFID systems provide certain advantages over conventional optical indicia recognition systems (e.g., bar code symbols). For example, the RFID transponders may have a memory capacity of several kilobytes or more, which is substantially greater than the maximum amount of data that may be contained in a bar code symbol. The RFID transponder memory may be re-written with new or additional data, which would not be possible with a printed bar code symbol. Moreover, RFID transponders may be

readable at a distance without requiring a direct line-of-sight view by the interrogator, unlike bar code symbols that must be within a direct line-of-sight and which may be entirely unreadable if the symbol is obscured or damaged. An additional advantage of RFID systems is that several RFID transponders may be read by the interrogator at one time.

As generally known in the art, an RFID tag or transponder may comprise a semiconductor chip and an antenna mounted to a substrate. This substrate may be enclosed (e.g., encapsulated, laminated, etc.) so that it is protected from the environment. It is known in the art to provide an RFID tag having a thin form factor, such as disclosed in U.S. Patent No. 5,528,222 issued to Moskowitz et al. For example, as shown in FIG. 1, a prior art RFID tag 100 may include an RF circuit chip 102 which is mounted in a flexible substrate 104. The chip 102 has electrical contacts 112 that are bonded at bond points 114 to an antenna 106 contained on the substrate 104. A window 108 is formed in the substrate 104 allowing the insertion of the chip 102 therein so that the thickness of the substrate 104 is not added to the thickness of the chip 102. The window 108 allows coating of the chip 102 with an encapsulant 110. The encapsulant 110 protects the chip 102 and the associated bonding structure 112, 114 from environmental exposure. The RFID tag 100 is sealed by thin flexible laminations 116 comprising an inner coating of hot melt adhesive 118 (such as ethyl-vinyl-acetate (EVA), phenolic butyral, or silicone adhesive) and an outer coating of tough polymeric material 120 (such as polyester, polyimide, or polyethylene). The antenna 106 (such as a resonant dipole, loop or folded dipole) is integrally formed on the substrate 104.

More particularly, the antenna 106 may comprise thin (e.g., 25 to 35 microns) copper lines which are etched onto a copper/organic laminate substrate or plated onto an organic substrate with a thickness (s). Typical materials used are polyester or polyimide for the organic substrate 104 and electroplated or rolled annealed copper for the antenna 106. The copper may further include gold and nickel plating to facilitate bonding. The chip

102 has a thickness (w), which may range from approximately 174 to 400 microns. In general, semiconductors are manufactured on thick wafers, e.g., up to 1 mm thick. The semiconductor may be made thinner by polishing or back grinding the wafer after manufacture. In the exemplary prior art RFID tag 100 of FIG. 1, the substrate 104 has a thickness (v) of approximately 225 microns or less, the bonding structure 112, 114 has a thickness (m) of approximately 50 microns, the laminating materials 116 have a thickness (u, q) of approximately 50 to 125 microns per side, and the encapsulate 110 above the antenna 106 and the substrate 104 has a thickness (r) of approximately 50 microns. Thus, the total thickness (t) of the prior art RFID tag 100 ranges from approximately 500 to 750 microns.

It is desirable to embed thin, flexible RFID tags in labels in both laminated and printed forms. Applications for such labels may include luggage or shipping tags used by airlines or other shippers to track the transportation of luggage and other packages or objects, wrist-band identification bracelets for tracking the movement of patients in a hospital, or animal collars for tracking the movement of animals such as household pets, farm animals, and the like. It is further desirable to use such labels in existing printers wherein the label embedded with the RFID tag is printed with indicia such as a barcode, alphanumeric characters or the like. While the prior art RFID tags described above already provide a thin form factor, the market continues to present packaging challenges to satisfy the demand for faster, smaller, and less expensive products. Accordingly, it is highly desirable to further reduce the form factor of an RFID tag.

SUMMARY OF THE INVENTION

Accordingly, the present invention is directed to packaging processes that provide RFID tags having reduced form factors and improved electrical performance. Moreover, the present invention provides RFID tags having both electrostatic discharge protection (ESD) and environmental protection in a thin form factor.

In a first embodiment of the invention, a radio frequency transponder comprises a substrate layer having an electrically conductive material disposed thereon, and a superstrate layer disposed above the substrate layer and having an integrated circuit retention aperture. The superstrate layer is laminated to the substrate layer and substantially covers the electrically conductive material on the substrate layer. An integrated circuit is substantially retained within the integrated circuit retention aperture and is operatively connected to the electrically conductive material. The substrate and superstrate layers may each be comprised of an organic material. The electrically conductive material comprises a metal patterned to provide an antenna. An encapsulant material is disposed within the integrated circuit retention aperture to substantially enclose the integrated circuit therein.

In a second embodiment of the invention, a radio frequency transponder comprises a substrate layer having an electrically conductive material disposed thereon and an integrated circuit retention aperture, a first superstrate layer disposed above the substrate layer and also having a integrated circuit retention aperture, and a second superstrate layer disposed below the substrate layer. The integrated circuit retention aperture of the substrate layer is disposed in substantial registration with the integrated circuit retention aperture of the first superstrate layer. The first and second superstrate layers are laminated together to provide a seal around the substrate layer. An integrated circuit is substantially retained within the integrated circuit retention apertures and is operatively connected to the electrically conductive material. An encapsulant is disposed within the integrated circuit apertures substantially enclosing the integrated circuit therein. The substrate layer may be comprised of a glass fabric impregnated with resin, and the superstrate layers may each be comprised of an organic material.

In a third embodiment of the invention, a radio frequency transponder comprises a substrate layer having an electrically conductive material disposed thereon and an integrated circuit retention aperture, and a

superstrate layer disposed below the substrate layer. The substrate and superstrate layers are laminated together. An integrated circuit is substantially retained within the integrated circuit retention aperture and is operatively connected to the electrically conductive material. An encapsulant is disposed within the integrated circuit aperture substantially enclosing the integrated circuit therein. The conductive material disposed on the substrate layer may be coated with an insulating material, such as a solder mask. The substrate layer may be comprised of a glass fabric impregnated with resin, and the superstrate layer may be comprised of an organic material.

It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory only and are not restrictive of the invention claimed. The accompanying drawings, which are incorporated in and constitute a part of the specification, illustrate an embodiment of the invention and together with the general description, serve to explain the principles of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

The numerous objects and advantages of the present invention may be better understood by those skilled in the art by reference to the accompanying figures in which:

FIG. 1 is a cross-sectional side elevational view showing a typical prior art thin RFID tag;

FIG. 2 is an isometric exploded view of an RFID tag including a perforated substrate according to a first embodiment of the present invention;

FIG. 3 is a cross-sectional side elevation view of the RFID tag of FIG. 2;

FIG. 4 is an isometric exploded view of an RFID tag including a chip-in-cavity structure according to a second embodiment of the present invention;

FIG. 5 is a cross-sectional side elevational view of the RFID tag of FIG. 4;

FIG. 6 is an isometric exploded view of an RFID tag including a chip-in-cavity structure according to a third embodiment of the present invention;

FIG. 7 is a cross-sectional side elevational view of the RFID tag of FIG. 6; and

FIG. 8 is a highly diagrammatic, isometric view of an exemplary process of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

The present invention satisfies the critical need for an RFID tag having a reduced form factor. In the detailed description that follows, it should be appreciated that like element numerals are used to describe like elements illustrated in one or more of the aforementioned figures.

Referring first to FIGS. 2 and 3, an RFID tag 10 having a chip-in-cavity (CIC) package constructed in accordance with a first embodiment of the invention is illustrated. The RFID tag 10 includes a substrate 12 and an upper superstrate 18 each comprised of an organic material such as polyimide or polyester. The substrate 12 includes an antenna 14 laminated thereon using a material having sufficiently high electrical conductivity, such as a metallic material comprising copper (Cu) or aluminum (Al). As known in the art, the antenna 14 may be patterned on the substrate 12 utilizing a photolithographic, ion etching, chemical etching, or vapor deposition process. The upper superstrate 18 includes an aperture 20 having a size and shape adapted to accommodate an integrated circuit 16 (described below). The upper superstrate 18 is then laminated on top of the substrate 12. Prior to this lamination step, any exposed metallic material may be selectively plated with, for example, electroless nickel (Ni) or gold (Au) in order to provide metallurgy, where needed, to facilitate electrical coupling between the antenna 14 and the integrated circuit 16 using known techniques, such as wire-bonding, tape automated bonding (TAB), or solder

reflow. Alternatively, where for example, the antenna 14 is comprised of copper (Cu), the copper traces may also be plated before the upper superstrate 18 is applied to the substrate 12. While the antenna 14 illustrated in FIG. 2 may be recognized as being a dipole antenna, it should be appreciated that other known types of antenna may be patterned on the substrate 12, such as a loop or folded dipole.

Once the substrate 12 and upper superstrate 18 have been laminated together, the integrated circuit 16 is operatively attached to the antenna 14, such as using bonds 22 (see, for example United States Patent No. 5,528,222, incorporated by reference herein). An encapsulating material 24, such as an epoxy, is then utilized to seal the integrated circuit 16 and protect the operative wire bonds 22. Preferably the aperture 20 in the upper superstrate 18 is slightly larger than the integrated circuit 16 so as to provide an annular space for the encapsulating material 24 to flow around the perimeter of the integrated circuit 16 (as shown in FIG. 3). The upper superstrate 18 serves as a mask for the substrate 12 in the process of selective plating onto the substrate 12 and/or shaping the encapsulating material 24. Moreover, the upper superstrate 18 serves to enhance protection of the RFID tag 10 from electrostatic discharge (ESD), moisture and other environmental hazards, and assists in controlling the shape of the encapsulating material 24.

FIGS. 4 and 5 illustrate an RFID tag 10' having chip-in-cavity (CIC) packaging constructed in accordance with a second embodiment of the present invention. The RFID tag 10' includes a substrate 32 comprised of either a flexible material such as described above, or a less flexible material such as a glass fabric impregnated with a resin (usually epoxy) generally used in the fabrication of printed circuit boards (e.g., FR-4) or ceramic. The substrate 32 includes an antenna 14 laminated thereon in the same manner as described above. An upper superstrate 18 and a lower superstrate 28 are each comprised of organic materials, such as described above. The upper superstrate 18 includes an aperture 20 having a size and shape

adapted to accommodate an integrated circuit 16, as also described above. The substrate 32 further includes an aperture 26 similar in shape and orientation as the aperture 20 of the upper superstrate 18, but slightly larger in dimensions. The aperture 26 of the substrate 32 is disposed in substantial alignment with the aperture 20 of the upper superstrate 18. The RFID tag 10' further includes a lower superstrate 28 disposed below the substrate 32.

The upper superstrate 18 and lower superstrate 28 are laminated together to hermetically seal the substrate 32 therein. An edge seal 30 is defined around the periphery of the upper and lower superstrates 18, 28 where the superstrate layers come into contact with each other (see FIG. 5). As described above, any exposed metallic material may be selectively plated with, for example, electroless nickel (Ni) or gold (Au) in order to provide metallurgy to permit coupling of the antenna 14 with the integrated circuit 16, such as using wire-bonding, tape automated bonding (TAB), or solder reflow techniques. Alternatively, where for example, the antenna 14 is comprised of copper (Cu), the copper traces may also be plated before the upper and lower superstrates 18, 28 are applied to the substrate 32. As noted above, FIG. 4 illustrates the antenna 14 as being a dipole antenna, but it should be appreciated that any known type of antenna may be advantageously utilized.

Once the upper and lower superstrates 18, 28 are laminated together to enclose the substrate 32, the integrated circuit 16 is placed on the lower superstrate 28 and is operatively attached to the antenna 14, such as using bonds 22. An encapsulating material 24, such as an epoxy, is then utilized to seal the integrated circuit 16 and protect the operative wire bonds 22. Preferably the apertures 20, 26 are slightly larger than the integrated circuit 16 so as to provide an annular space for the encapsulating material 24 to flow around the perimeter of the integrated circuit 16 (as shown in FIG. 5). As described above, the upper superstrate 18 serves as a mask for the substrate 32 in selectively plating onto the substrate and/or shaping the encapsulating material 24. Moreover, the upper and lower superstrates 18, 28 serve to enhance protection of the RFID tag 10' from electrostatic

discharge (ESD), moisture and other environmental hazards, and assists in controlling the shape of the encapsulating material 24.

FIGS. 6 and 7 illustrate an RFID tag 10" having chip-in-cavity (CIC) packaging constructed in accordance with a third embodiment of the present invention. The RFID tag 10" includes a substrate 32 comprised of either a flexible material such as described above, or a less flexible material such as a glass fabric impregnated with a resin (usually epoxy) generally used in the fabrication of printed circuit boards (e.g., FR-4) or ceramic. The substrate 32 includes an antenna 14 laminated thereon in the same manner as described above. A lower superstrate 28 is comprised of organic materials, such as described above. The substrate 32 includes an aperture 26 having a size and shape adapted to accommodate an integrated circuit 16, as also described above.

Unlike the preceding embodiment, an upper superstrate is not included in this embodiment. Instead, the antenna 14 is coated with an insulating material, such as a solder mask comprised of polymer materials. The substrate 32 and the lower superstrate 28 are then laminated together. Any unmasked metallic material may be selectively plated with electroless nickel (Ni) or gold (Au) in order to provide metallurgy to permit coupling of the antenna 14 with the integrated circuit 16, such as using wire-bonding, tape automated bonding (TAB), or solder reflow techniques. Alternatively, where for example, the antenna 14 is comprised of copper (Cu), the copper traces may also be plated. As noted above, FIG. 6 illustrates the antenna 14 as being a dipole antenna, but it should be appreciated that any known type of antenna may be advantageously utilized.

Thereafter, the integrated circuit 16 is placed on the lower superstrate 28 and is operatively attached to the antenna 14, such as using bonds 22. An encapsulating material 24, such as an epoxy, is then utilized to seal the integrated circuit 16 and protect the operative wire bonds 22. Preferably the aperture 26 is slightly larger than the integrated circuit 16 so as to provide an annular space for the encapsulating material 24 to flow around the perimeter

of the integrated circuit 16 (as shown in FIG. 7). As described above, the lower superstrate 28 serves to enhance protection of the RFID tag 10" from electrostatic discharge (ESD), moisture and other environmental hazards, and assists in controlling the shape of the encapsulating material 24.

FIG. 8 illustrates a process for fabricating RFID tags 10' in accordance with the embodiment of the present invention described above with respect to FIGS. 4 and 5. The exemplary process is used to fabricate a reel 40 of finished RFID tags 10', which may be indexed with indexing sprocket holes. For specific applications, such as insertion into labels, such a process is advantageous in a high speed automated processing system. Even though the following process is described in connection with RFID tags 10' as illustrated in FIGS. 4 and 5, it should be appreciated that a similar process may be used to fabricate RFID tags 10 as illustrated in FIGS. 2 and 3, and RFID tags 10" as illustrated in FIGS. 6 and 7. In addition, it should also be appreciated that a similar process can be used to fabricate RFID tags 10, 10', 10" in finished formats other than reels, such as sheets, panels, etc.

In the automated process of FIG. 8, the upper and lower superstrates 18, 28 and substrate 32 are laminated together to provide a continuous web (such as a 35 mm film strip format or the like), with sprocket holes defined along outer edges of the web. As described above, the substrate 32 includes an antenna 14 formed from electrically conductive materials and an aperture 26, and the upper superstrate 18 includes an aperture 20 disposed in substantial alignment with the aperture 26. More particularly, the lower superstrate 28 may be provided first as a base layer, with the substrate 32 deposited onto the lower superstrate. The antenna 14 may then be patterned onto the exposed substrate 32. Next, the upper superstrate 18 is deposited onto the substrate 32, and the three successive layers are laminated together to form a single web of material. An integrated circuit 16 may then be placed (via suitable automation apparatus 34) within the apertures 20, 26 and electrically connected to the antenna 14. An

encapsulant 24 may then be applied (via suitable automation apparatus 36), which flows around the integrated circuit 16. Upon curing of the encapsulant 24, the continuous reel 40 may be segmented into individual RFID tag products.

It is believed that the integrated circuit attachment process and apparatus of the present invention and many of its attendant advantages will be understood by the foregoing description, and it will be apparent that various changes may be made in the form, construction and arrangement of the components thereof without departing from the scope and spirit of the invention or without sacrificing all of its material advantages. The form herein before described being merely an explanatory embodiment thereof, it is the intention of the following claims to encompass and include any such changes.

CLAIMS

What is claimed is:

1. A radio frequency transponder, comprising:

a substrate having an electrically conductive material disposed on a first surface thereof;

at least one superstrate coupled to at least one of said first surface of said substrate and a second surface of said substrate;

an integrated circuit retention aperture provided by at least one of said substrate and said at least one superstrate; and

an integrated circuit substantially retained within said integrated circuit retention aperture and operatively connected to said electrically conductive material.

2. The radio frequency transponder of Claim 1, wherein said at least one superstrate is comprised of an organic material.

3. The radio frequency transponder of Claim 1, wherein said electrically conductive material comprises metal.

4. The radio frequency transponder of Claim 1, wherein said electrically conductive material further comprises an antenna.

5. The radio frequency transponder of Claim 1, wherein said at least one superstrate further comprises a first superstrate coupled to said first surface of said substrate and a second superstrate coupled to said second surface of said substrate, and said integrated circuit retention aperture is defined by apertures provided in both said substrate and said first superstrate.

6. The radio frequency transponder of Claim 5, wherein said first superstrate and said second superstrate are coupled together to provide a seal around said substrate.

7. The radio frequency transponder of Claim 1, wherein said at least one superstrate further comprises a first superstrate coupled to said second surface of said substrate, and said integrated circuit retention aperture is defined by an aperture provided in said substrate.

8. The radio frequency transponder of Claim 1, wherein said at least one superstrate further comprises a first superstrate coupled to said first surface of said substrate, and said integrated circuit retention aperture is defined by an aperture provided in said first superstrate.

9. The radio frequency transponder of Claim 1, further comprising an encapsulant disposed within said integrated circuit retention aperture substantially enclosing said integrated circuit therein.

10. The radio frequency transponder of Claim 9, wherein said encapsulant further comprises epoxy.

11. The radio frequency transponder of Claim 1, wherein said substrate is comprised of a glass fabric impregnated with resin.

12. The radio frequency transponder of Claim 1, wherein said substrate is comprised of an organic material.

13. The radio frequency transponder of Claim 1, wherein said integrated circuit further comprises a radio frequency identification circuit.

14. A method of fabricating a radio frequency transponder, comprising the steps of:

providing a substrate having an electrically conductive material disposed on a first surface thereon, and at least one superstrate;

defining an integrated circuit retention aperture in at least one of said substrate and said at least one superstrate;

laminating said at least one superstrate onto at least one of said first surface of said substrate and a second surface of said substrate;

disposing an integrated circuit within said integrated circuit retention aperture and operatively connecting said integrated circuit to said electrically conductive material; and

encapsulating said integrated circuit within said integrated circuit retention aperture using an encapsulant material.

15. The method of Claim 14, wherein said providing step further comprises providing said at least one superstrate from an organic material.

16. The method of Claim 14, further comprising the step of patterning an antenna on said substrate from said electrically conductive material.

17. The method of Claim 14, wherein said at least one superstrate further comprises a first and second superstrate, and said laminating step further comprises laminating said first superstrate to said first surface of said substrate and laminating said second superstrate to said second surface of said substrate.

18. The method of Claim 17, wherein said defining step further comprises defining said integrated circuit retention aperture in both said substrate and said first superstrate in substantial registration therewith.

19. The method of Claim 18, wherein said laminating step further comprises laminating said first and second superstrates together to form a seal around said substrate.

20. The method of Claim 14, wherein said at least one superstrate further comprises a single superstrate, and said laminating step further comprises laminating said superstrate to said second surface of said substrate.

21. The method of Claim 20, wherein said wherein said defining step further comprises defining said integrated circuit retention aperture in said substrate only.

22. The method of Claim 14, wherein said at least one superstrate further comprises a single superstrate, and said laminating step further comprises laminating said superstrate to said first surface of said substrate.

23. The method of Claim 22, wherein said wherein said defining step further comprises defining said integrated circuit retention aperture in said superstrate only.

24. The method of Claim 14, wherein said encapsulating step further comprises using an epoxy as said encapsulant material.

25. The method of Claim 14, further comprising the step of selectively plating within said integrated circuit retention aperture to provide bonding points for operatively connecting said integrated circuit to said electrically conductive material.

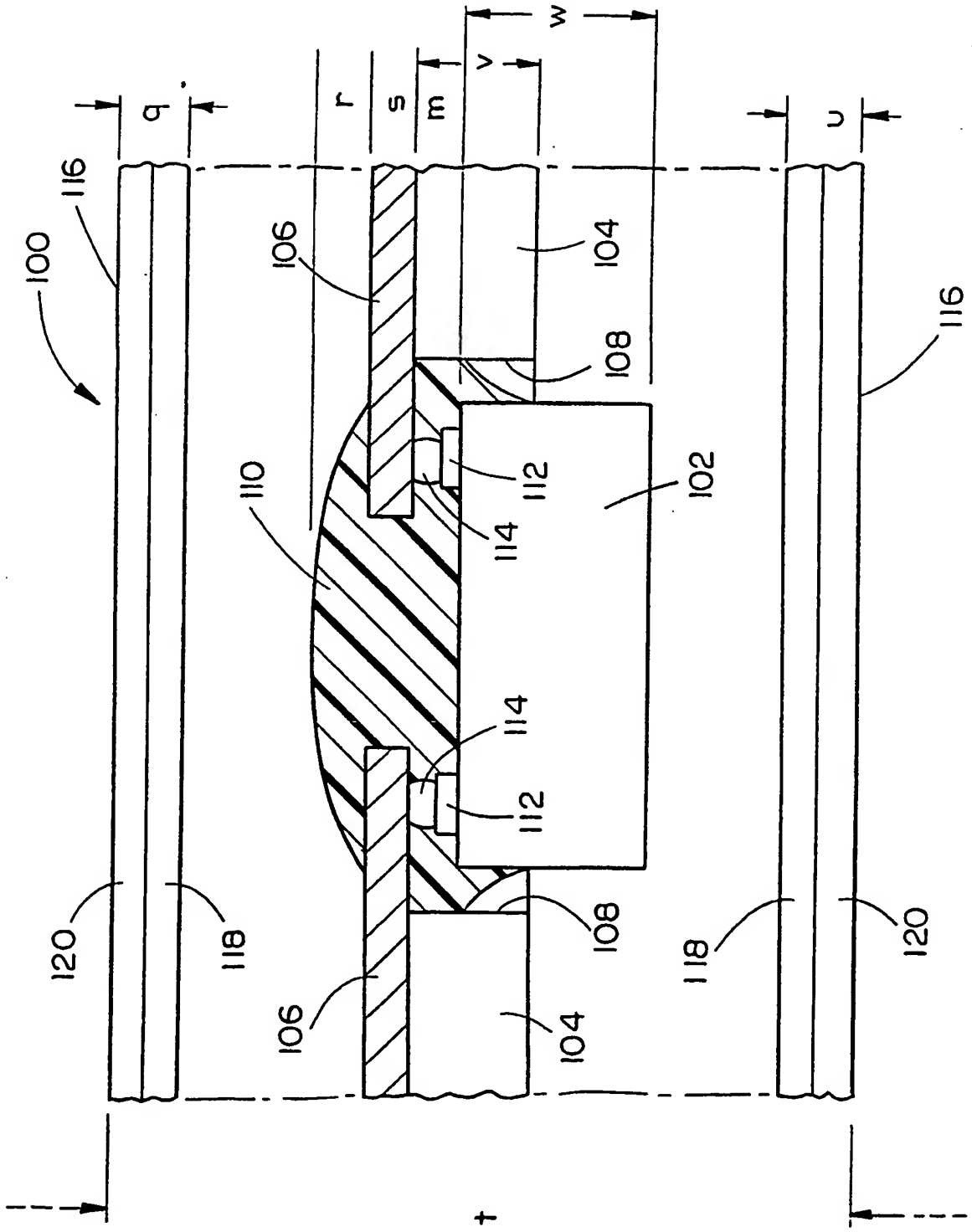


FIG. 1
(PRIOR ART)

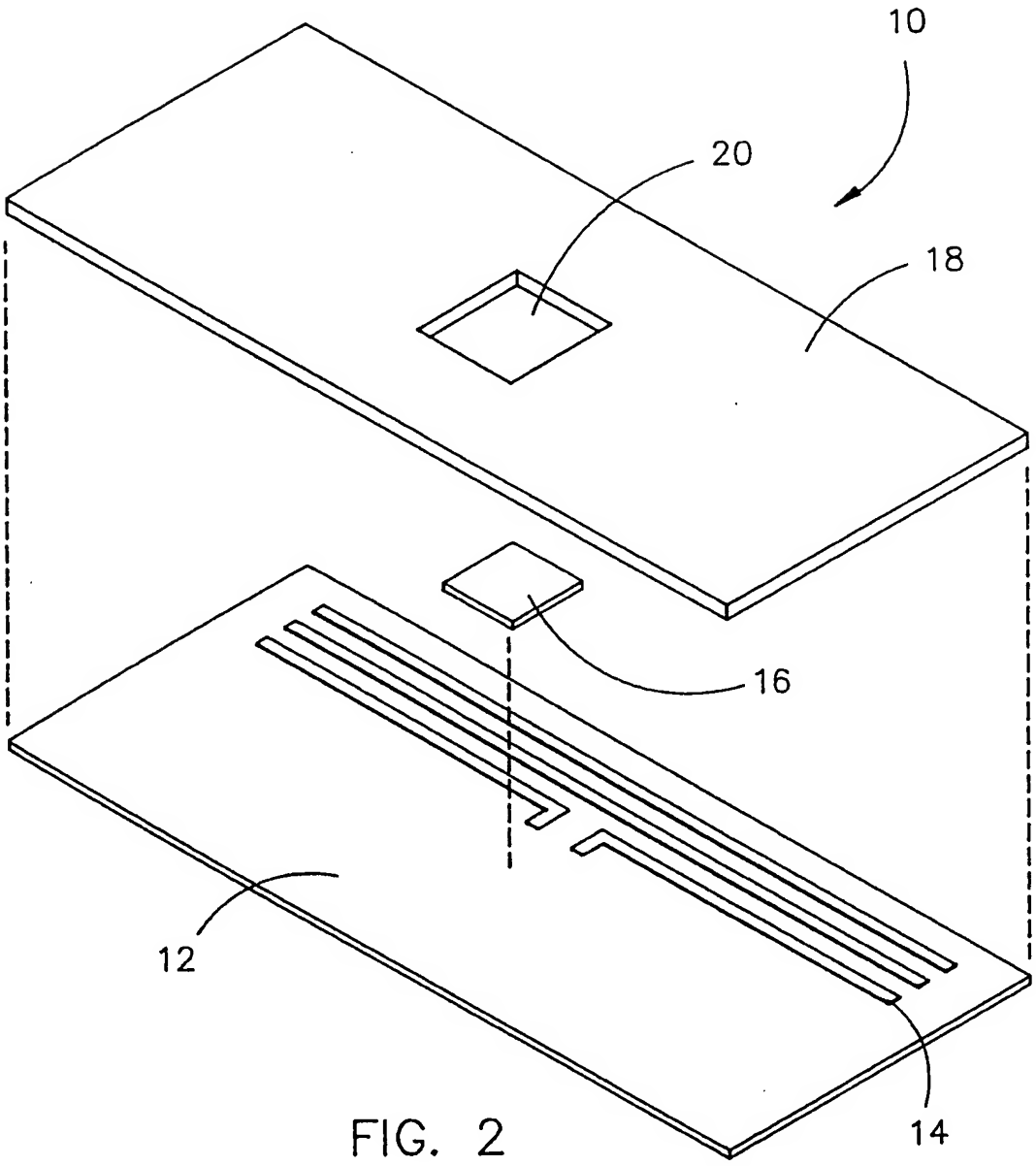


FIG. 2

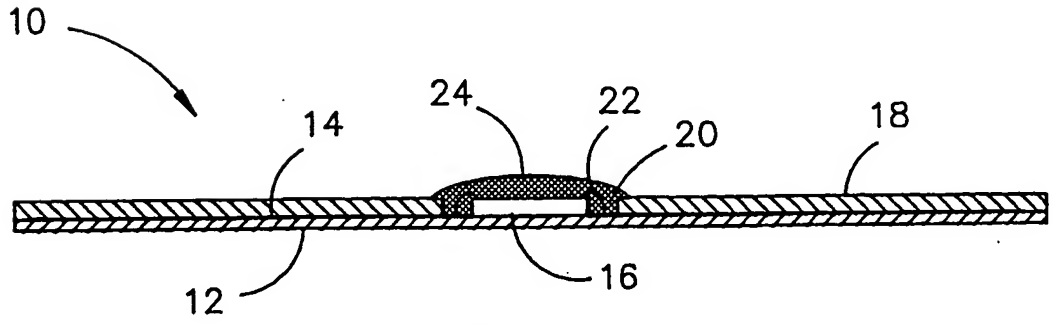


FIG. 3

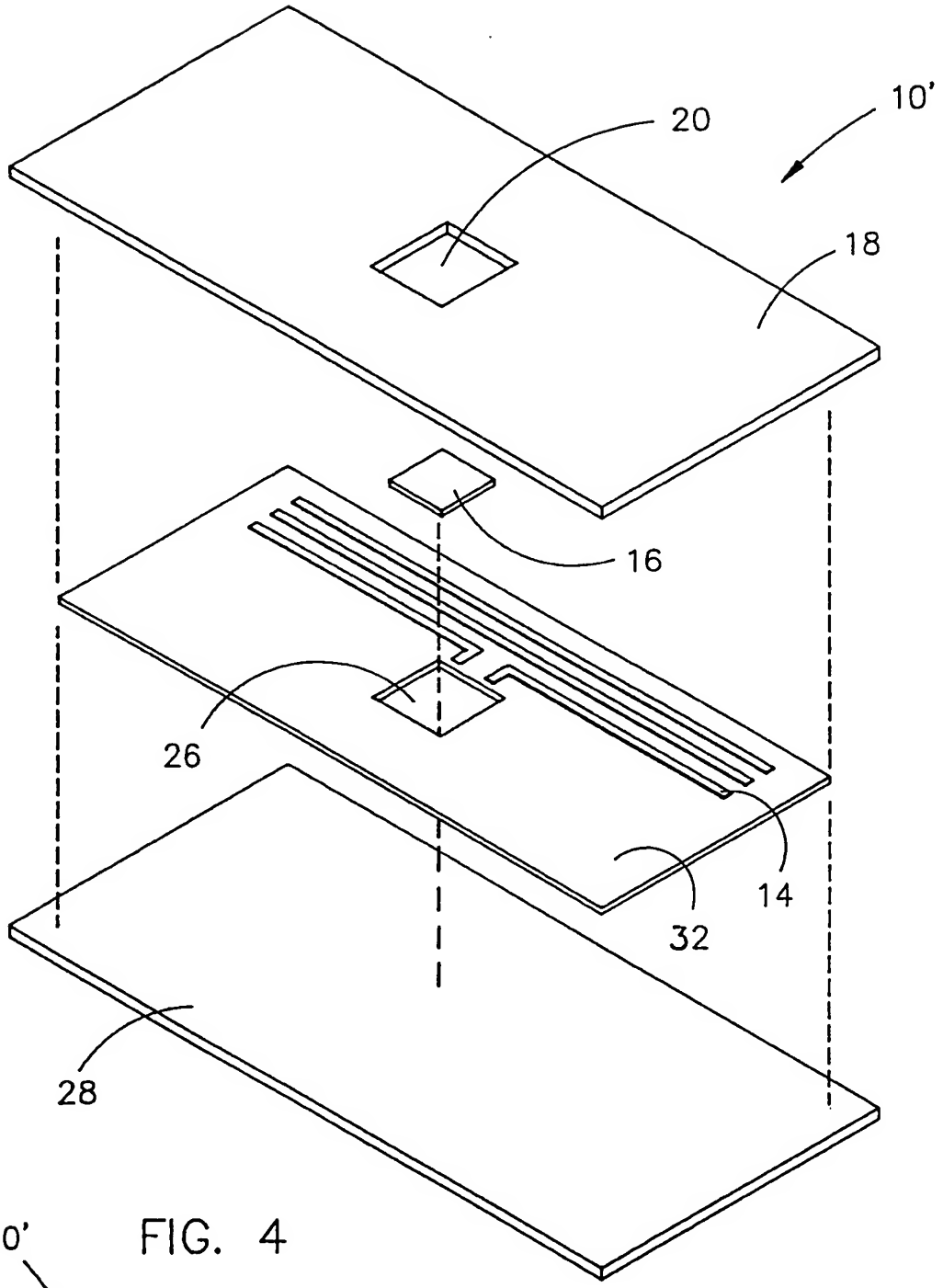


FIG. 4

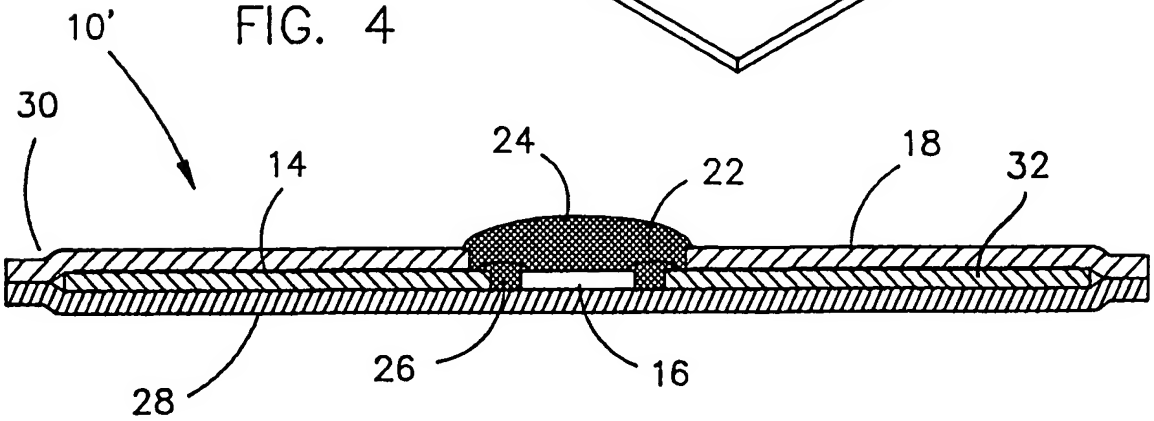


FIG. 5

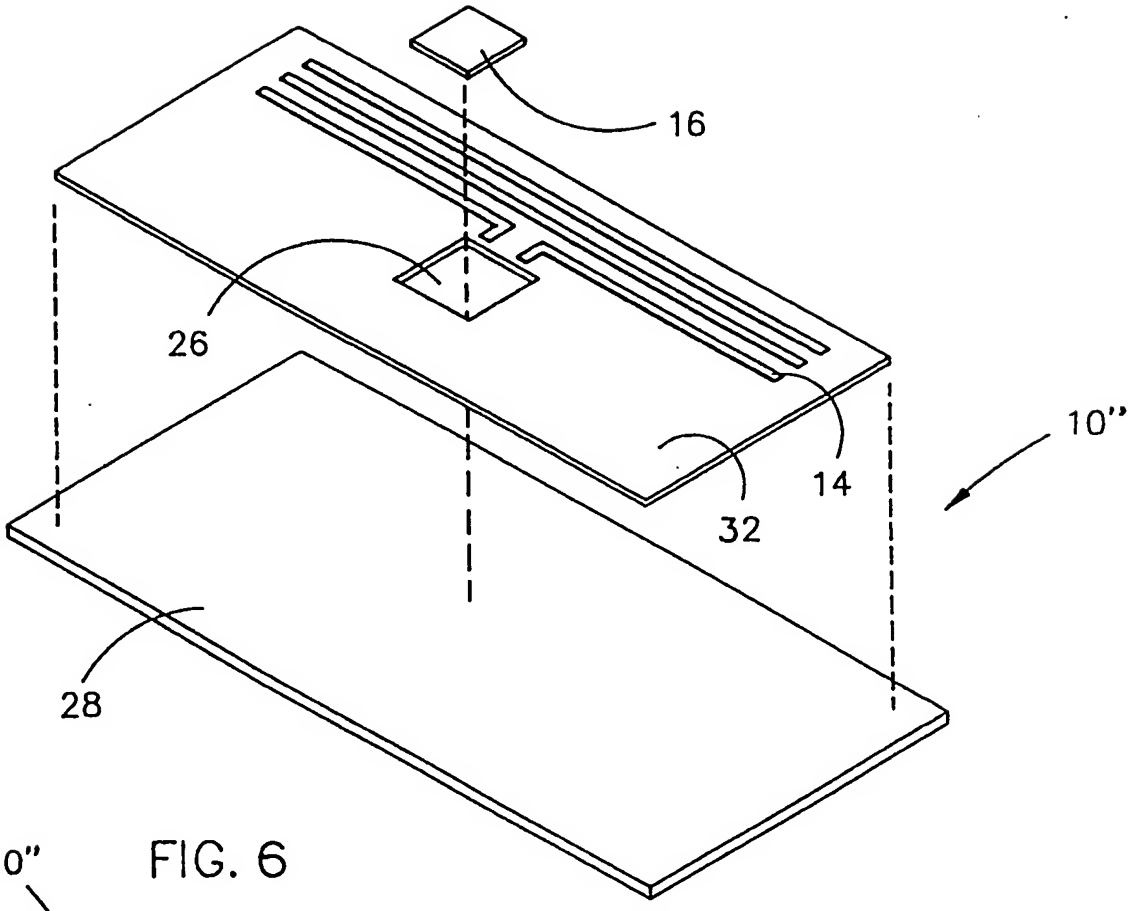


FIG. 6

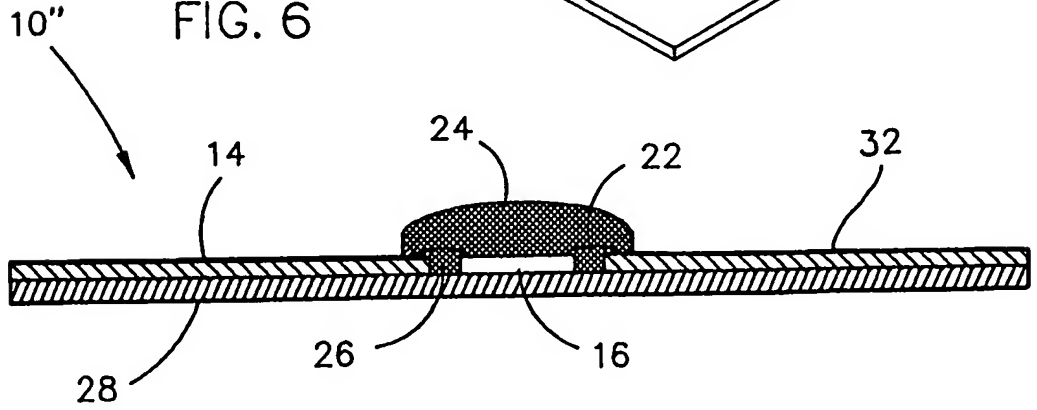


FIG. 7

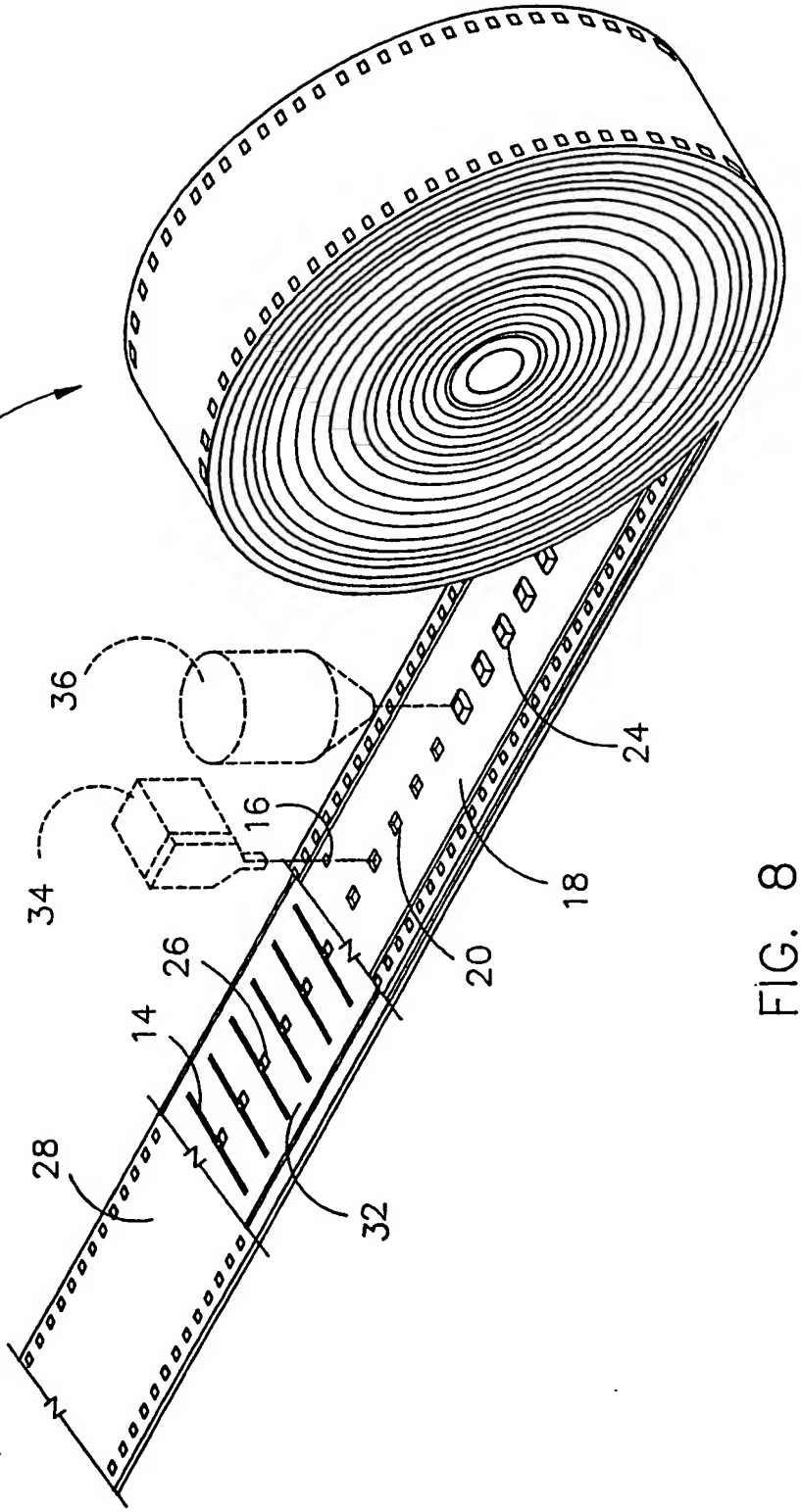


FIG. 8

INTERNATIONAL SEARCH REPORT

Inter nal Application No
PCT/US 99/22438

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L23/66 H01L23/64

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	EP 0 595 549 A (HUGHES MICROELECTRONICS EUROPA) 4 May 1994 (1994-05-04)	1
A	claims 1,12,17; figures 3,8	2-4, 12-16
Y	DE 196 48 308 A (MURATA MANUFACTURING CO) 22 May 1997 (1997-05-22)	1
A	column 3, line 44 -column 4, line 32; figure 5	5,7
A	FR 2 745 119 A (THOMSON CSF) 22 August 1997 (1997-08-22) claims 1,12,16	4,16,24

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
13 April 2000	26/04/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	De Raeve, R

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Inten ..nal Application No
PCT/US 99/22438

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT *

Category *	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 528 222 A (COTEUS PAUL W ET AL) 18 June 1996 (1996-06-18) cited in the application column 4, line 61 -column 5, line 21; figure 3	1-3,7,12
A	WO 94 18700 A (INDALA CORP) 18 August 1994 (1994-08-18) claim 1	1

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

Inten nal Application No
PCT/US 99/22438

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0595549 A	04-05-1994	DE 69313776 D	16-10-1997
		DE 69313776 T	19-02-1998
		JP 6243358 A	02-09-1994
DE 19648308 A	22-05-1997	JP 9148373 A	06-06-1997
		GB 2307596 A	28-05-1997
FR 2745119 A	22-08-1997	NONE	
US 5528222 A	18-06-1996	AT 179270 T	15-05-1999
		CA 2153441 A	10-03-1996
		CN 1118910 A	20-03-1996
		DE 69509242 D	27-05-1999
		DE 69509242 T	04-11-1999
		WO 9607985 A	14-03-1996
		EP 0780007 A	25-06-1997
		EP 0855675 A	29-07-1998
		HU 76996 A	28-01-1998
		JP 8088586 A	02-04-1996
		KR 191975 B	15-06-1999
		PL 318977 A	21-07-1997
		SG 46938 A	20-03-1998
		ZA 9507078 A	11-03-1996
WO 9418700 A	18-08-1994	US 5420757 A	30-05-1995
		AU 673423 B	07-11-1996
		AU 6394394 A	29-08-1994
		CA 2155208 A	18-08-1994
		EP 0683923 A	29-11-1995
		JP 8506708 T	16-07-1996